CLAIMS

WHAT IS CLAIMED IS:

1. An electronic tester, comprising:

a test head coupled to a device under test, wherein the device under test can be system-on-a-chip integrated circuit, a mixed signal integrated circuit, a digital integrated circuit, or an analog integrated circuit;

digital test circuitry that applies digital test signals to the device under test coupled to the test head and receives digital outputs from the device under test in response to the digital test signals;

analog test circuitry that applies analog test signals to the device under test coupled to the test head and receives analog outputs from the device under test in response to the analog test signals;

memory test circuitry that applies memory test patterns to the device under test coupled to the test head and receives memory outputs from the device under test in response to the memory test.

a tester computer that supervises the application of digital, analog, and memory test signals from the digital test circuitry, analog test circuitry, and memory test circuitry to the device under test such that signals applied to the device under test can be solely digital test signals, solely analog test signals, solely memory test signals, or mixed digital, analog, and memory test signals,

wherein the test head, the digital test circuitry, the analog test circuitry, the memory test circuitry, and the computer are operable as a single platform.

2. The electronic tester of claim 1, wherein the memory test circuitry comprises an algorithmic pattern generator.

3. The electronic tester of claim 2, wherein the memory test circuitry further comprises a fail log memory.

4. The electronic tester of claim 1, wherein the digital test circuitry comprises a control pattern memory processing unit and a data pattern memory processing unit.

5. The electronic tester of claim 1, wherein the analog test circuitry comprises a sequenced measure system.

6. The electronic tester of claim 1, wherein the analog test circuitry comprises a pulsed power source.

7. The electronic tester of claim 5, wherein the analog test circuitry further comprises vector radio frequency circuitry.

8. The electronic tester of claim 1, wherein the digital test circuitry, the analog test circuitry, and the memory test circuitry are modular and reconfigurable.

9. The electronic tester of claim 1, wherein the digital test signals, the analog test signals, and the memory test patterns can be applied concurrently to the device under test.

10. An electronic tester, comprising:

means for applying digital test signals to a device under test and receiving digital outputs from the device under test in response to the digital test signals;

means for applying analog test signals to the device under test and receiving analog outputs from the device under test in response to the analog test signals;

means for applying memory test patterns to the device under test and receiving memory outputs from the device under test in response to the memory test patterns;

computing means for supervising the application of digital, analog, and memory test signals to the device under test by the means for applying digital test signals, analog test signals, and memory test patterns, wherein the device under test can be a system-on-a-chip integrated circuit, a mixed signal integrated circuit, a digital integrated circuit, an analog integrated circuit, or a memory integrated circuit, wherein the means for applying digital test signals, the means for applying analog test signals, the means for applying memory test patterns, and the computing means are coupled to a single platform.

11. An electronic tester, comprising:

analog test circuitry that applies analog test signals to a device under test coupled to a test head and receives analog outputs from the device under test in response to the analog test signals;

a tester controller that sends action packets to the analog test circuitry for setting voltages of pins of the test head;

digital test circuitry that applies digital test signals to the device under test coupled to the test head and receives digital outputs from the device under test in response to the digital test signals;

memory test circuitry that applies memory test patterns to the device under test coupled to the test head and receives memory outputs from the device under test in response to the memory test;

a computer coupled to the tester controller, the digital test circuitry, and the memory test circuitry wherein the computer causes the tester controller to send action packets to the analog test circuitry to execute analog tests of the device under test, wherein the computer causes the digital test circuitry to execute digital tests of the device under test, and wherein the computer causes the memory test circuitry to execute memory tests with respect to the device under test.

12. A method for an electronic tester, comprising the steps of:

presenting to a user of the electronic tester a computer-generated graphical user interface for launching an operating system for the electronic

tester, wherein the operating system can execute digital test programs, and analog test programs, and memory test programs for testing a device under test coupled to the electronic tester;

launching the operating system in response to user input via the computer-generated graphical user interface.

13. A method of executing tests on an electronic tester, comprising the steps of:

presenting to a user of the electronic tester a computer-generated graphical user interface for starting a digital test program component to be followed automatically by an analog test program component, wherein the digital and analog test program components test a device under test coupled to a test head of the electronic tester;

receiving an input from the user to start the digital test program component;

executing the digital test program component with respect to the device under test;

automatically executing the analog test program component following completion of the digital test program component.

14. A method of executing tests on an electronic tester, comprising the steps of:

presenting to a user of the electronic tester a computer-generated graphical user interface for starting an analog test program component to be followed automatically by a digital test program, wherein the analog and digital test program components test a device under test coupled to a test head of the electronic tester;

receiving an input from the user to start the analog test program component;

executing the analog test program component with respect to the device under test;

automatically executing the digital test program component following completion of the analog test program component.

15. A method of arranging program flow on an electronic tester, comprising the steps of:

presenting to the user of the electronic tester a computer-generated graphical user interface that displays program icons representing digital test program components and analog test program components for testing a device under test coupled to a test head of the electronic tester;

presenting to the user of the electronic tester in the computer-generated graphical user interface controls that allow the user to arrange a sequence of program execution by linking program icons, wherein a program icon representing a digital test program component can be directly linked to a

program icon representing an analog test program component to create an automatic sequence of program execution between a digital test program component and an analog test program component.

16. A method of displaying program flow on an electronic tester, comprising the steps of:

presenting to the user of the electronic tester a computer-generated graphical user interface that displays program icons representing digital test program components and analog test program components for testing a device under test coupled to a test head of the electronic tester;

presenting to the user of the electronic tester in the computer-generated graphical user interface a display of links with respect to the program icons, wherein at least one program icon representing a digital test program component is directly linked to a program icon representing an analog test program component.

17. A method for an electronic tester, comprising the steps of:

presenting to the user of the electronic tester a computer-generated object representing an analog test procedure with respect to a device under test coupled to the electronic tester;

presenting to the user a computer-generated object representing a digital test procedure with respect to the device under test;

presenting to the user a computer-generated graphical user interface that allows the user to display source code of the analog test procedure in response to selection of the analog test procedure object by the user;

presenting to the user a computer-generated graphical user interface that allows the user to display source code of the digital test procedure in response to the selection of the digital test procedure object by the user.

18. A method for debugging code of an electronic tester, comprising the steps of:

presenting to a user of the electronic tester a computer-generated object representing an analog test procedure with respect to a device under test coupled to the electronic tester;

presenting to the user a computer-generated object representing a digital test procedure with respect to the device under test;

presenting to the user a computer-generated graphical user interface for debugging the analog test procedure in response to selection of the analog test procedure object by the user;

presenting to the user a computer-generated graphical user interface for debugging the digital test procedure in response to selection of the digital test procedure object by the user.

19. A method for an electronic tester, comprising the steps of:

stepping through a program sequence of a digital test program component for testing a device under test coupled to the electronic tester;

calling an analog test procedure for testing the device under test from within the digital test program component while stepping through the digital test program component;

executing the analog test procedure with respect to the device under test;

continuing stepping through the program sequence of the digital test program component after calling the analog test procedure.

20. A method for an electronic tester, comprising:

stepping through a program sequence of an analog test program component for testing a device under test coupled to the electronic tester;

calling a digital test program component for testing the device under test from within the analog test program while stepping through the analog test program;

executing the digital test program component with respect to the device under test;

continuing stepping through the program sequence of the analog test program component after calling the digital test program component.

21. A method for controlling timing on an electronic tester, comprising the steps of:

having a master of the electronic tester send a timing marker over a marker bus of the electronic tester;

having a modular test circuit of the electronic tester retrieve the timing marker from the marker bus;

having the modular test circuit start a test on a device under test coupled to the electronic tester upon receipt of the timing marker, wherein the test is controlled by a test sequence predefined for the modular test circuit prior to retrieval of the timing marker by the modular test circuit.

22. The method of claim 21, further comprising the step of having the modular test circuit send a completion marker on the marker bus to the master upon completion of the test by the modular test circuit, wherein the completion marker indicates to the master completion of the test by the modular test circuit.

23. The method of claim 21, wherein the timing marker is a digital signal and wherein the test is an analog test.

24. The method of claim 21, further comprising the steps of:

having a second modular test circuit of the electronic tester retrieve the timing marker from the marker bus;

having the second modular test circuit start a second test on the device under test upon receipt of the timing marker, wherein the second test is controlled by a second test sequence predefined for the second modular test circuit prior to retrieval of the timing marker by the second modular test circuit.

25. An electronic tester, comprising:

a test head;

a master that generates a timing marker;

as marker bus coupled to the master;

a modular test circuit that retrieves the timing marker from the marker bus, wherein the modular test circuit starts a test with respect to the test head upon receipt of the timing marker, wherein the test is controlled by a test sequence predefined for the modular test circuit prior to retrieval of the timing marker by the modular test circuit.

26. A clocking apparatus for an electronic tester, comprising:

a first high speed clock generator coupled to a digital test circuit, wherein the first high speed clock generator generates a first clock having a first frequency that is a first multiple of an input frequency;

a second high speed clock generator coupled to an analog test circuit, wherein the second high speed clock generator generates a second clock having a second frequency that is a second multiple of the input frequency;

a reference frequency clock source;

a variable clock generator coupled the reference frequency clock source and coupled to the first and second high speed clock generators, wherein the variable clock generator has a continuously adjustable clock frequency that

determines the input frequency for the first and second high speed clock generators.

27. The clocking apparatus of claim 26, further comprising a computer that sets the clock frequency of the variable frequency clock generator in response to user input with respect to the computer.

28. The clocking apparatus of claim 26, wherein the reference frequency clock source provides a reference clock for a clock for an analog test circuit.

29. The clocking apparatus of claim 26, wherein the first and second multiples are each less than one.

30. The clocking apparatus of claim 26, wherein the first and second multiples are each greater than one.